IN THE CLAIMS:

Claims 1-3, and 5-22 have been amended herein. All of the pending claims 1 through 22 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A semiconductor device assembly, comprising:

a first semiconductor device including a surface with a plurality of peripherally located bond pads;

a rerouting element positioned over ~~said~~ the first semiconductor device, ~~said~~ the rerouting element comprising:

a base substrate;

a plurality of conductive vias positioned adjacent at least two peripheral edges of ~~said~~ the base substrate, each conductive via of ~~said~~ the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad of the first semiconductor device upon assembly of ~~said~~ the rerouting element with the first semiconductor device;

a plurality of conductive traces; and

a plurality of rerouted bond pads, each conductive trace of ~~said~~ the plurality of conductive traces extending from a corresponding conductive via of the plurality of conductive vias toward at least one other peripheral edge of ~~said~~ the base substrate to a corresponding rerouted bond pad of ~~said~~ the plurality of rerouted bond pads; and

a second semiconductor device positioned over a portion of ~~said~~ the rerouting element, each of ~~said~~ the plurality of rerouted bond pads being exposed beyond a periphery of ~~said~~ the rerouting element.

2. (Currently Amended) The semiconductor device assembly of claim 1, wherein each rerouted bond pad of ~~said~~ the plurality of rerouted bond pads is located laterally adjacent a periphery of ~~said~~ the first semiconductor device.

3. (Currently Amended) The semiconductor device assembly of claim 1, wherein each rerouted bond pad of ~~said~~ the plurality of rerouted bond pads is located adjacent a single edge of ~~said~~ the first semiconductor device.

4. (Original) The semiconductor device assembly of claim 1, further comprising: a carrier substrate.

5. (Currently Amended) The semiconductor device assembly of claim 4, wherein ~~said~~ the first semiconductor device is secured to ~~said~~ the carrier substrate.

6. (Currently Amended) The semiconductor device assembly of claim 4, wherein ~~said~~ the carrier substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

7. (Currently Amended) The semiconductor device assembly of claim 4, wherein ~~said~~ the at least one rerouted bond pad is in communication with a corresponding contact area of ~~said~~ the carrier substrate.

8. (Currently Amended) The semiconductor device assembly of claim 7, further comprising:
a discrete conductive element positioned between ~~said~~ the at least one rerouted bond pad and ~~said~~ the corresponding contact area.

9. (Currently Amended) The semiconductor device assembly of claim 8, wherein ~~said~~ the ~~at least one~~ discrete conductive element comprises at least one of a bond wire, a tape-automated bond element trace, and a lead.

10. (Currently Amended) The semiconductor device assembly of claim 1, further comprising:

another rerouting element on a bond pad-bearing surface of ~~said~~ the second semiconductor device.

11. (Currently Amended) The semiconductor device assembly of claim 1, wherein ~~said~~ the second semiconductor device is oriented in staggered relation to ~~said~~ the first semiconductor device.

12. (Currently Amended) The semiconductor device assembly of claim 1, wherein ~~said~~ the second semiconductor device is smaller than ~~said~~ the first semiconductor device.

13. (Currently Amended) The semiconductor device assembly of claim 1, further comprising:

at least one additional semiconductor device positioned over ~~said~~ the second semiconductor device.

14. (Currently Amended) The semiconductor device assembly of claim 8, further comprising:

an encapsulant protecting at least portions of ~~said~~ the first semiconductor device, ~~said~~ the second semiconductor device, ~~said~~ the ~~at least one~~ discrete conductive element, and portions of ~~said~~ the carrier substrate located laterally adjacent outer peripheries of ~~said~~ the first and second semiconductor devices.

15. (Currently Amended) The semiconductor device assembly of claim 14, wherein ~~said~~ the encapsulant comprises a glob-top type encapsulant.

16. (Currently Amended) The semiconductor device assembly of claim 14, wherein ~~said~~ the encapsulant comprises a transfer molding compound.

17. (Currently Amended) The semiconductor device assembly of claim 14, further comprising:

at least one external connective element in communication with at least one bond pad of ~~said~~ the first semiconductor device.

18. (Currently Amended) A rerouting element for use with a semiconductor device, comprising:

a base substrate;

a plurality of conductive vias positioned adjacent at least two peripheral edges of ~~said~~ the base substrate, each conductive via of ~~said~~ the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad of the semiconductor device upon assembly of ~~said~~ the rerouting element with the semiconductor device;

a plurality of conductive traces; and

a plurality of contact pads, each conductive trace of ~~said~~ the plurality of conductive traces extending from a corresponding conductive via toward at least one other peripheral edge of ~~said~~ the base substrate to a corresponding contact pad of ~~said~~ the plurality of contact pads.

19. (Currently Amended) The rerouting element of claim 18, wherein ~~said~~ the plurality of conductive vias are positioned adjacent three peripheral edges of ~~said~~ the base substrate.

20. (Currently Amended) The rerouting element of claim 19, wherein each contact pad of ~~said~~ the plurality of contact pads is positioned adjacent to another, single peripheral edge of ~~said~~ the base substrate.

21. (Currently Amended) The rerouting element of claim 18, wherein ~~said~~ the plurality of conductive vias are positioned adjacent to two adjacent peripheral edges of ~~said~~ the base substrate.

22. (Currently Amended) The rerouting element of claim 21, wherein each contact pad of ~~said~~ the plurality of contact pads is positioned adjacent to at least one of two other adjacent peripheral edges of ~~said~~ the base substrate.